CS5560

±2.5 V / 5 V, 50 kSps, 24-bit, High-throughput $\Delta\Sigma$ ADC

Features

- Differential Analog Input
- On-chip Buffers for High Input Impedance
- Conversion Time = 20 µS
- Settles in One Conversion
- Linearity Error = 0.0007%
- Signal-to-Noise = 110 dB
- 24 Bits, No Missing Codes
- Self-calibration:
  - Maintains accuracy over time & temperature.
- Simple three/four-wire serial interface
- Power Supply Configurations:
  - Analog: +5V/GND; IO: +1.8V to +3.3V
  - Analog: ±2.5V; IO: +1.8V to +3.3V
- Power Consumption:
  - ADC Input Buffers On: 85 mW
  - ADC Input Buffers Off: 70 mW

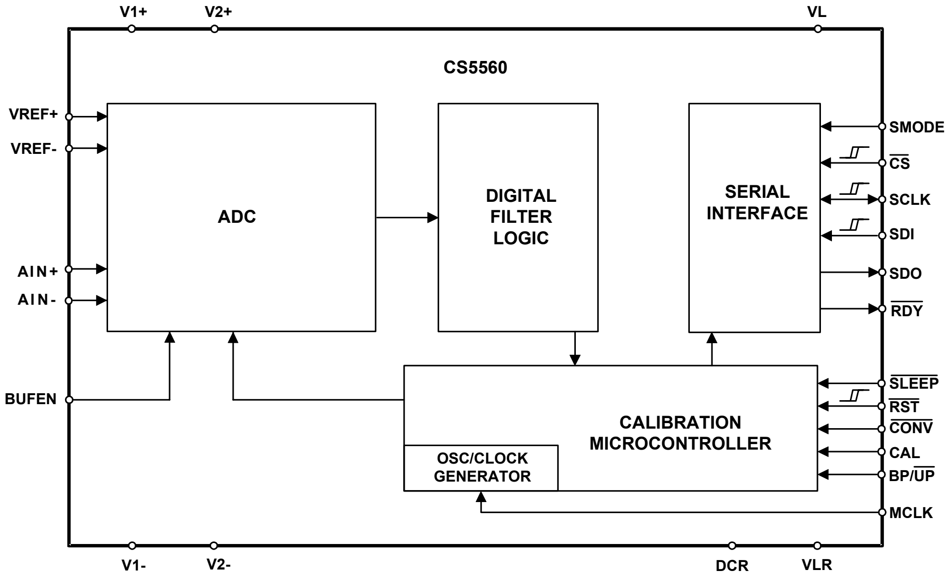
General Description

The CS5560 is a single-channel, 24-bit analog-to-digital converter capable of 50 kSps conversion rate. The input accepts a fully differential analog input signal. On-chip buffers provide high input impedance for both the AIN inputs and the VREF+ input. This significantly reduces the drive requirements of signal sources and reduces errors due to source impedances. The CS5560 is a delta-sigma converter capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion. The converter's 24-bit data output is in serial form, with the serial port acting as either a master or a slave. The converter is designed to support bipolar, ground-referenced signals when operated from ±2.5V analog supplies.

The CS5560 uses self-calibration to achieve low offset and gain errors. The converter achieves a S/N of 110 dB. Linearity is ±0.0007% of full scale.

The converter can operate from an analog supply of 0-5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

ORDERING INFORMATION:
See *Ordering Information* on page 32.



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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the specified operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VLR = 0 V. All voltages with respect to 0 V.

ANALOG CHARACTERISTICS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL. BUFEN = V1+ unless otherwise stated. Connected per Figure 7. Bipolar mode unless otherwise stated.

Parameter		Min	Typ	Max	Unit
Accuracy					
Linearity Error (Note 1)		-	0.0003	-	±%FS
Differential Linearity Error (Note 2)		-	±0.1	-	LSB_{24}
Positive Full-scale Error	After Reset After Calibration (Note 1)	- -	1.0 0.01	-	%FS
Negative Full-scale Error	After Reset After Calibration (Note 1)	- -	1.0 0.01	-	%FS
Full-scale Drift (Note 3)		-		-	LSB_{24}
Unipolar Offset	After Reset After Calibration (Note 1)	- -	±2000 ±400	- -	LSB_{24}
Unipolar Offset Drift (Note 3)		-		-	LSB_{24}
Bipolar Offset	After Reset After Calibration (Note 1)	- -	±1000 ±200	- -	LSB_{24}
Bipolar Offset Drift (Note 3)		-		-	LSB_{24}
Noise		-	9.5	-	µVrms
Dynamic Performance					
Peak Harmonic or Spurious Noise	1 kHz, -0.5 dB Input	-	-110	-	dB
Total Harmonic Distortion	1 kHz, -0.5 dB Input	-	-110	-	dB
Signal-to-Noise		-	110	-	dB
S/(N + D) Ratio	-0.5 dB Input, 1 kHz -60 dB Input, 1 kHz	- -	107 48	- -	dB dB
-3 dB Input Bandwidth (Note 4)		-	42	-	kHz

1. Applies after calibration at any temperature within -40 °C to +85 °C.
2. No missing codes is guaranteed at 24 bits resolution over the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up, at 25° C.
4. Scales with MCLK.

ANALOG CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL.; BUFEN = V1+ unless otherwise stated. Connected per Figure 7.

Parameter		Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Unipolar	0 to +VREF			V
	Bipolar	±VREF			V
Input Capacitance		-	10	-	pF
CVF Current (Note 5)	AIN Buffer On (BUFEN = V+)	-	600	-	nA
	AIN Buffer Off (BUFEN = V-)	-	130	-	µA
	ACOM	-	130	-	µA
Voltage Reference Input					
Voltage Reference Input Range (VREF+) – (VREF-)	(Note 6)	2.4	4.096	4.2	V
Input Capacitance		-	10	-	pF
CVF Current	VREF+ Buffer On (BUFEN = V+)	-	3	-	µA
	VREF+ Buffer Off (BUFEN = V-)	-	1	-	mA
	VREF-	-	1	-	mA
Power Supplies					
DC Power Supply Currents	I_{V1}	-	-	18	mA
	I_{V2}	-	-	1.8	mA
	I_{VL}	-	-	0.5	mA
Power Consumption	Normal Operation Buffers On	-	85	105	mW
	Buffers Off	-	70	90	mW
Power Supply Rejection (Note 7)	V1+ , V2+ Supplies	90	110	-	dB
	V1-, V2- Supplies	90	110	-	dB

5. Measured using an input signal of 1 V DC.
6. For optimum performance, VREF+ should always be less than (V+) - 0.2 volts to prevent saturation of the VREF+ input buffer.
7. Tested with 100 mVP-P on any supply up to 1 kHz. V1+ and V2+ supplies at the same voltage potential, V1- and V2- supplies at the same voltage potential.

SWITCHING CHARACTERISTICS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator External Clock	XIN f_{clk}	12 0.5	14 16	16 16.2	MHz MHz
Master Clock Duty Cycle			40	-	60	%
Reset						
$\overline{\text{RST}}$ Low Time		t_{res}	1	-	-	µs
$\overline{\text{RST}}$ rising to $\overline{\text{RDY}}$ falling	Internal Oscillator External Clock	t_{wup}	- -	120 1536	- -	µs MCLKs
Calibration						
CAL pulse width	(Note 8)	t_{pw}	4	-	-	MCLKs
CAL high setup time to $\overline{\text{RST}}$ rising	(Note 8)	t_{ccw}	0	-	-	ns
Calibration Time $\overline{\text{RST}}$ rising (CAL high) to $\overline{\text{RDY}}$ falling		t_{scl}	-	331458	-	MCLKs
Calibration Time CAL rising ($\overline{\text{RST}}$ high) to $\overline{\text{RDY}}$ falling		t_{cal}	-	331458	-	MCLKs
Conversion						
$\overline{\text{CONV}}$ Pulse Width		t_{cpw}	4	-	-	MCLKs
BP/$\overline{\text{UP}}$ setup to $\overline{\text{CONV}}$ falling	(Note 9)	t_{scn}	0	-	-	ns
$\overline{\text{CONV}}$ low to start of conversion		t_{scn}	-	-	2	MCLKs
Perform Single Conversion ($\overline{\text{CONV}}$ high before $\overline{\text{RDY}}$ falling)		t_{bus}	20	-	-	MCLKs
Conversion Time	(Note 10) Start of Conversion to $\overline{\text{RDY}}$ falling	t_{buh}	-	-	324	MCLKs
Sleep Mode	$\overline{\text{SLEEP}}$ low to low-power state $\overline{\text{SLEEP}}$ high to device active (Note 11)	t_{con} t_{con}	- -	50 3083	- -	µs MCLKs

8. CAL can be controlled by the same signal used for $\overline{\text{RST}}$. If CAL goes high simultaneously with $\overline{\text{RST}}$, a calibration will be performed, but CAL must remain high until $\overline{\text{RDY}}$ falls.
9. BP/$\overline{\text{UP}}$ can be changed coincident $\overline{\text{CONV}}$ falling. BP/$\overline{\text{UP}}$ must remain stable until $\overline{\text{RDY}}$ falls.
10. If $\overline{\text{CONV}}$ is held low continuously, conversions occur every 320 MCLK cycles.
    If $\overline{\text{RDY}}$ is tied to $\overline{\text{CONV}}$, conversions will occur every 322 MCLKs.
    If $\overline{\text{CONV}}$ is operated asynchronously to MCLK, a conversion may take up to 324 MCLKs.
    $\overline{\text{RDY}}$ falls at the end of conversion.
11. $\overline{\text{RDY}}$ will fall when the device is fully operational when coming out of sleep mode.

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
$\overline{\text{RDY}}$ falling to MSB stable	t_1	-	-2	-	MCLKs
Data hold time after SCLK rising	t_2	-	10	-	ns
Serial Clock (Out) (Note 12, 13) Pulse Width (low)	t_3	50	-	-	ns
Pulse Width (high)	t_4	50	-	-	ns
$\overline{\text{RDY}}$ rising after last SCLK rising	t_5	-	8	-	MCLKs

12. SDO and SCLK will be high impedance when $\overline{\text{CS}}$ is high. In some systems it may require a pull-down resister.
13. SCLK = MCLK/2.

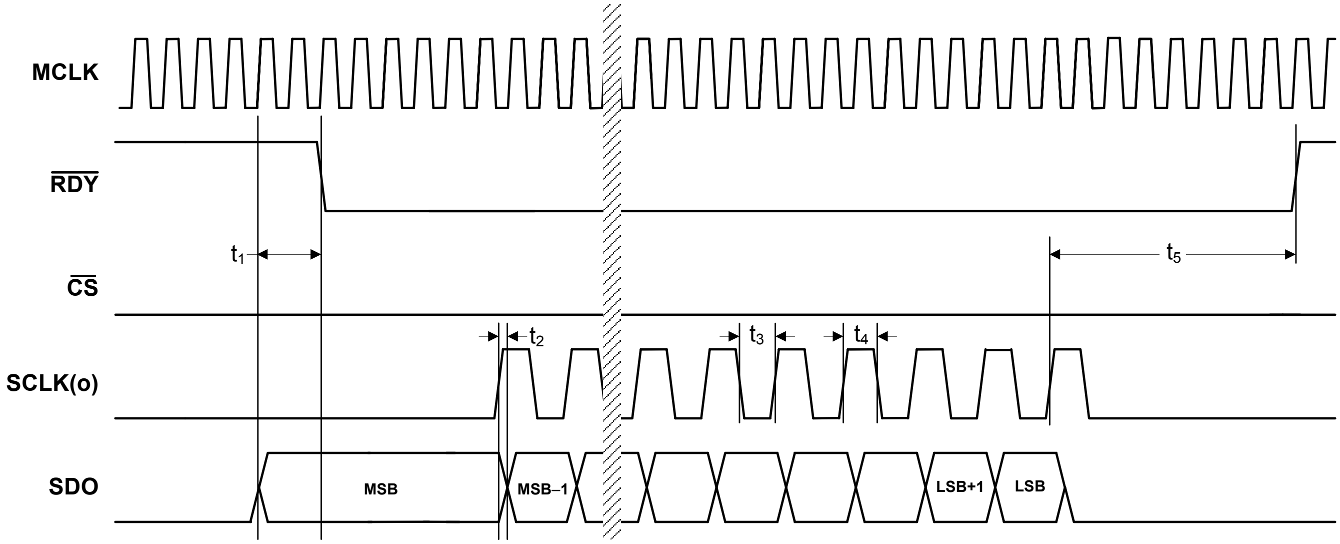


Figure 1. SSC Mode - Read Timing, $\overline{\text{CS}}$ remaining low (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)						
Data hold time after SCLK rising		t_7	-	10	-	ns
Serial Clock (Out) (Note 14, 15)	Pulse Width (low) Pulse Width (high)	t_8 t_9	50 50	- -	- -	ns ns
$\overline{\text{RDY}}$ rising after last SCLK rising		t_{10}	-	8	-	MCLKs
$\overline{\text{CS}}$ falling to MSB stable		t_{11}	-	10	-	ns
First SCLK rising after $\overline{\text{CS}}$ falling		t_{12}	-	8	-	MCLKs
$\overline{\text{CS}}$ hold time (low) after SCLK rising		t_{13}	10	-	-	ns
SCLK, SDO tristate after $\overline{\text{CS}}$ rising		t_{14}	-	5	-	ns

14. SDO and SCLK will be high impedance when $\overline{\text{CS}}$ is high. In some systems it may require a pull-down resister.
15. SCLK = MCLK/2.

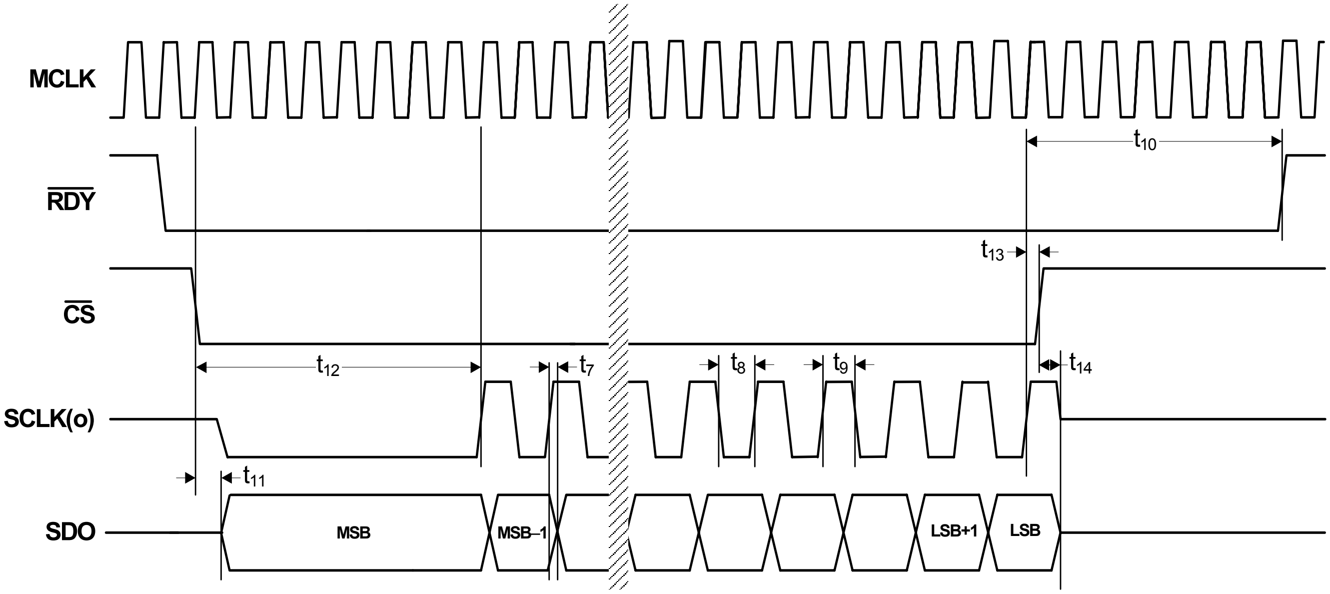


Figure 2. SSC Mode - Read Timing, $\overline{\text{CS}}$ falling after $\overline{\text{RDY}}$ falls (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SEC Mode (SMODE = VLR)					
SCLK(in) Pulse Width (High)	-	30	-	-	ns
SCLK(in) Pulse Width (Low)	-	30	-	-	ns
$\overline{\text{CS}}$ hold time (high) after $\overline{\text{RDY}}$ falling	t_{15}	10	-	-	ns
$\overline{\text{CS}}$ hold time (high) after SCLK rising	t_{16}	10	-	-	ns
$\overline{\text{CS}}$ low to SDO out of Hi-Z (Note 16)	t_{17}	-	10	-	ns
Data hold time after SCLK rising	t_{18}	-	10	-	ns
Data setup time before SCLK rising	t_{19}	10	-	-	ns
$\overline{\text{CS}}$ hold time (low) after SCLK rising	t_{20}	10	-	-	ns
$\overline{\text{RDY}}$ rising after SCLK falling	t_{21}	-	10	-	ns

16. SDO will be high impedance when $\overline{\text{CS}}$ is high. In some systems it may require a pull-down resistor.

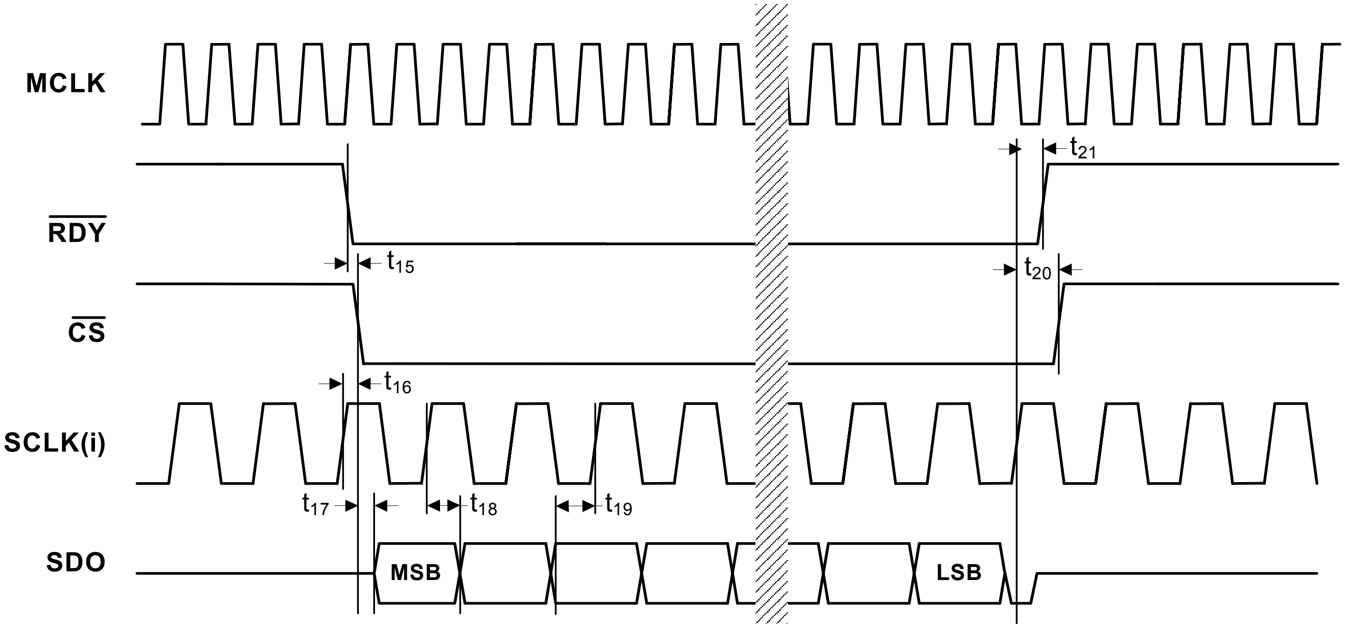


Figure 3. SEC Mode - Read Timing (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Calibration Register Read Timing					
$\overline{\text{CS}}$ hold time (high) after SCLK rising	t_{22}	10	-		ns
Data setup time before SCLK rising	t_{23}	10	-	-	ns
Data hold time after SCLK rising	t_{24}	10	-	-	ns
SCLK rising to data stable	t_{25}	-	10	-	ns
Data hold time after SCLK rising	t_{26}	-	10	-	ns
SCLK rising to $\overline{\text{CS}}$ rising	t_{27}	10	-	-	ns
SDO tristate after $\overline{\text{CS}}$ rising	t_{28}	-	5	-	ns

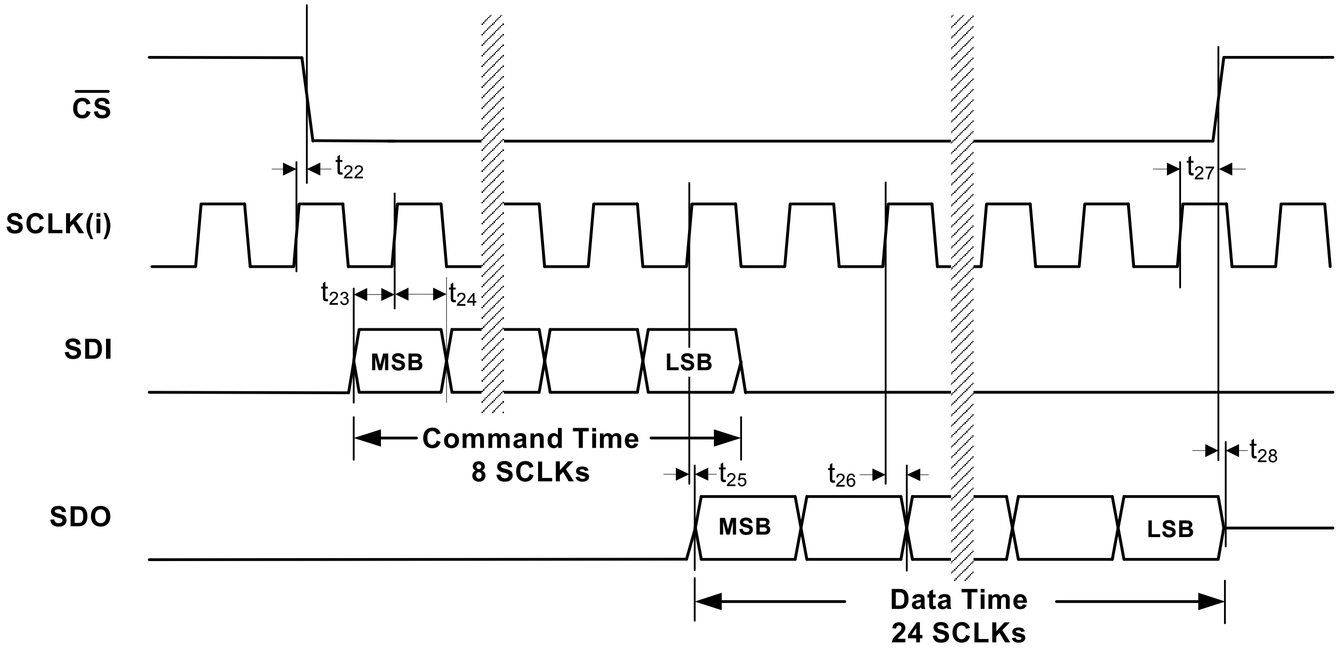


Figure 4. SEC Mode - Calibration Register Read Timing (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Calibration Register Write Timing					
Data setup time before SCLK rising	t_{29}	10	-	-	ns
Data hold time after SCLK rising	t_{30}	10	-	-	ns
SCLK rising to $\overline{CS}$ rising	t_{31}	10	-	-	ns

17. SDO will be high impedance when $\overline{CS}$ is high. In some systems it may require a pull-down resister.

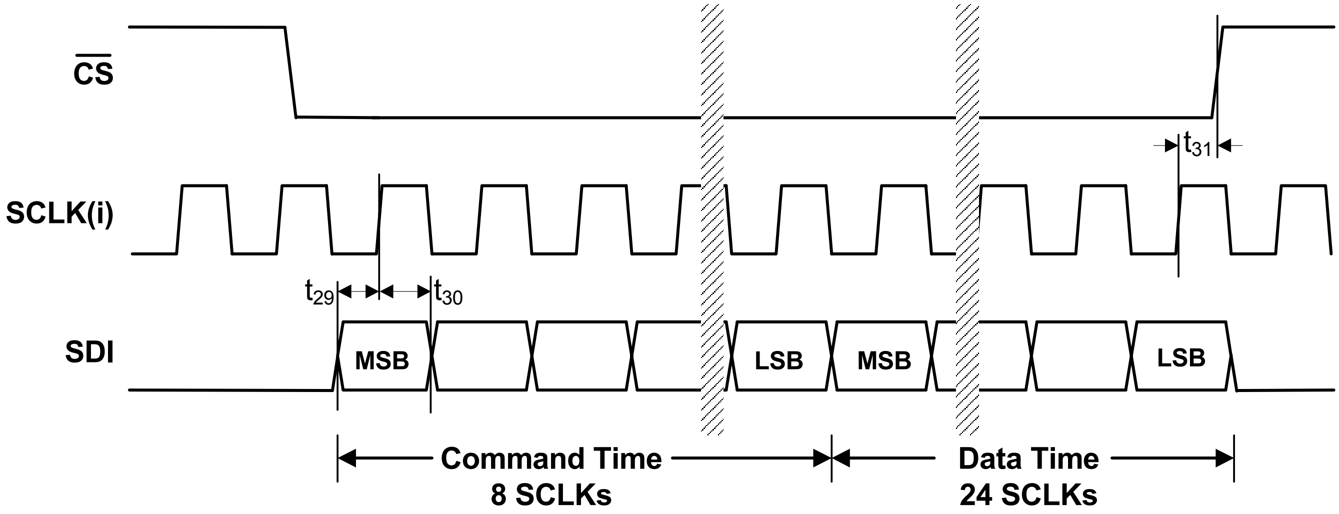


Figure 5. SEC Mode - Write Timing (Not to Scale)

DIGITAL CHARACTERISTICS

T_A = TMIN to TMAX; VL = 3.3V, ±5% or VL = 2.5V, ±5% or 1.8V, ±5%; VLR = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Calibration Memory Retention (Note 18) Power Supply Voltage [V1+ = V2+] – [V1- = V2-]	V_{MR}	4.0	-	-	V
Input Leakage Current	I_{in}	-	-	2	µA
Digital Input Pin Capacitance	C_{in}	-	3	-	pF
Digital Output Pin Capacitance	C_{out}	-	3	-	pF

18. VA- and VD- can be any value from 0 to +5V for memory retention. Neither VA- nor VD- should be allowed to go positive. AIN1, AIN2, or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.

DIGITAL FILTER CHARACTERISTICS

T_A = TMIN to TMAX; VL = 3.3V, ±5% or VL = 2.5V, ±5% or 1.8V, ±5%; VLR = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Group Delay	-	-	160	-	MCLKs

GUARANTEED LOGIC LEVELS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V; Logic 1 = VD+; CL = 15 pF.

			Guaranteed Limits				
Parameter	**Sym**	**VL**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Logic Inputs							
Minimum High-level Input Voltage:	V_{IH}	3.3	1.9			V	
		2.5	1.6				
		1.8	1.2				
Maximum Low-level Input Voltage:	V_{IL}	3.3			1.1	V	
		2.5			0.95		
		1.8			0.6		
Logic Outputs							
Minimum High-level Output Voltage:	V_{OH}	3.3	2.9			V	I_{OH} = -2 mA
		2.5	2.1				
		1.8	1.65				
Maximum Low-level Output Voltage:	V_{OL}	3.3			0.36	V	I_{OH} = -2 mA
		2.5			0.36		
		1.8			0.44		

RECOMMENDED OPERATING CONDITIONS

(VLR = 0V, see Note 19)

Parameter		Symbol	Min	Typ	Max	Unit
Single Analog Supply						
DC Power Supplies:	(Note 19)					
	V1+	V1+	4.75	5.0	5.25	V
	V2+	V2-	4.75	5.0	5.25	V
	V1-	V1+	-	0	-	V
	V2-	V2-	-	0	-	V
Dual Analog Supplies						
DC Power Supplies:	(Note 19)					
	V1+	V1+	+2.375	+2.5	+2.625	V
	V2+	V2-	+2.375	+2.5	+2.625	V
	V1-	V1+	-2.375	-2.5	-2.625	V
	V2-	V2-	-2.375	-2.5	-2.625	V
Analog Reference Voltage	(Note 20) [VREF+] – [VREF-]	VREF	2.4	4.096	4.2	V

19. The logic supply can be any value VL – VLR = +1.6 to +3.6 volts as long as VLR ≥ V2- and VL ≤ 3.6 V.
20. The differential voltage reference magnitude is constrained by the V1+ or V1- supply magnitude.

ABSOLUTE MAXIMUM RATINGS

(VLR = 0V)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:						
	[V1+] – [V1-] (Note 21)	-	0	-	5.5	V
	VL + [|V1-|] (Note 22)	-	0	-	6.3	V
Input Current, Any Pin Except Supplies	(Note 23)	I_{IN}	-	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)	V_{INA}	(V1-) – 0.3	-	(V1+) + 0.3	V
Digital Input Voltage		V_{IND}	VLR – 0.3	-	VL + 0.3	V
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. V1+ = V2+; V1- = V2-
22. V1- = V2-
23. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation beyond these limits may result in permanent damage to the device.

2. OVERVIEW

The CS5560 is a 24-bit analog-to-digital converter capable of 50 kSps conversion rate. The device is capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion.

The converter is a serial output device. The serial port can be configured to function as either a master or a slave.

The CS5560 provides self-calibration circuitry to achieve low offset and gain errors.

The converter can operate from an analog supply of 5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

The CS5560 converts at 50 kSps when operating from a 16 MHz input clock.

3. THEORY OF OPERATION

The CS5560 converter provides high-performance measurement of DC or AC signals. The converter includes on-chip calibration circuitry to minimize offset and gain errors. The converter can be used to perform single conversions or continuous conversions upon command. Each conversion is independent of previous conversions and can settle to full specified accuracy, even with a full-scale input voltage step. This is due to the converter architecture which uses a combination of a high-speed delta-sigma modulator and a low-latency filter architecture.

Once power is established to the converter, a reset must be performed. A reset initializes the internal converter logic and sets the offset register to zero and the gain register to a decimal value of 1.0. If the $\overline{\mathrm{CAL}}$ pin is low when $\overline{\mathrm{RST}}$ transitions from low to high, no calibration will be performed. If CAL is high when $\overline{\mathrm{RST}}$ goes high, the converter's offset & gain slope will be calibrated.

If $\overline{\mathrm{CONV}}$ is held low then the converter will convert continuously with $\overline{\mathrm{RDY}}$ falling every 320 MCLKs. This is equivalent to 50 kSps if MCLK = 16.0 MHz. If $\overline{\mathrm{CONV}}$ is tied to $\overline{\mathrm{RDY}}$, a conversion will occur every 322 MCLKs. If $\overline{\mathrm{CONV}}$ is operated asynchronously to MCLK, it may take up to 324 MCLKs from $\overline{\mathrm{CONV}}$ falling to $\overline{\mathrm{RDY}}$ falling.

Multiple converters can operate synchronously if they are driven by the same MCLK source and $\overline{\mathrm{CONV}}$ to each converter falls on the same MCLK falling edge. Alternately, $\overline{\mathrm{CONV}}$ can be held low and all devices are reset with $\overline{\mathrm{RST}}$ rising on the same falling edge of MCLK.

The output coding of the conversion word is a function of the BP/$\overline{\mathrm{UP}}$ pin.

The active-low $\overline{\mathrm{SLEEP}}$ signal causes the device to enter a low-power state. The calibration register contents are preserved during sleep. When exiting sleep, the converter will take 3083 MCLK cycles before conversions can be performed. $\overline{\mathrm{RST}}$ should remain inactive (high) when $\overline{\mathrm{SLEEP}}$ is asserted (low).

3.1 Reset and Calibration

After the power supplies and the voltage reference are stable, the converter must be reset. The reset function initializes the internal logic in the converter, but does not initiate calibration. After reset has been performed, the converter can be used uncalibrated, or calibration can be performed. Calibration minimizes offset and gain errors inside the converter. If the device is used without calibration, conversions will include the offset and gain errors of the uncalibrated converter, but the converter will maintain its differential and integral linearity. Calibration of offset and gain can be performed upon command.

Calibration can be initiated in either of two ways. If CAL is high when $\overline{\text{RST}}$ transitions from low to high, a calibration cycle will be performed. When calibration is performed, the offset and full-scale points of the converter are calibrated. A calibration cycle takes 327,680 MCLK cycles. The $\overline{\text{RDY}}$ signal falls upon completion of reset and calibration sequence. If CAL is held low when $\overline{\text{RST}}$ transitions from low to high, no calibration will be performed. Calibrations can be initiated any time the converter is idle by taking the CAL input high. $\overline{\text{RDY}}$ will fall at the end of the calibration cycle. The CAL pin should be returned low when not being used.

A calibration cycle calibrates the offset and full-scale points of the converter transfer function. When the offset portion of the calibration is performed, the AIN+ and AIN- pins are disconnected from the input and shorted internally. The offset of the converter is then measured and a correction factor is stored in the offset calibration register. Then the voltage reference is internally connected to act as the input signal to the converter and a gain calibration is performed. The gain correction results are placed in the gain calibration register. The contents of the 24-bit offset and gain registers are used to map the conversion data prior to its output from the converter. The offset and gain calibration registers can be read and written if desired. To read or write the calibration registers inside of the converter, the converter must be idle, and the serial port must be in the SEC mode (SMODE = VLR). Table 1 depicts the commands necessary to read or write the calibration registers.

Table 1. Offset & Gain Calibration Register Read/Write Commands

Register	Read Command	Write Command
Offset Register	0x40	0xC0
Gain Register	0x20	0XA0

3.1.1 Offset Register

MSB	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
Sign	2^{-2}										2^{-12}
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB
2^{-11}											2^{-24}
0	0	0	0	0	0	0	0	0	0	0	0

The offset register maps one for one with the conversion word when the gain register is set to 1 decimal. After reset all bits are zero.

3.1.2 Gain Register

MSB	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13
2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
0	0	1	0	0	0	0	0	0	0	0	0

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	LSB
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}
0	0	0	0	0	0	0	0	0	0	0	0

The gain register spans from 0 to ($8 - 2^{-21}$). After reset, bit D22 is 1, all others are 0. This results in a decimal gain value of 1.000....000.

The on-chip calibration registers can be read or written via the serial port. Reading or writing into the calibration registers requires that the serial port be in the SEC mode. To write into the offset or gain register, the appropriate 8-bit command (see Table 1 on page 16) is first shifted into the SDI pin. Rising edges of SCLK latch the bits. To perform a write, the 8-bit command is immediately followed by the 24 bit data word to be written. When a read command is used, the 24 bit data word from the register will be output from the SDO pin. The data bits will be output on rising edges of SCLK. The data bits have sufficient hold time to be latched externally by the next rising edge of SCLK.

3.2 Conversion

The CS5560 converts at 50 kSps when synchronously operated ($\overline{\text{CONV}}$ = VLR) from a 16.0 MHz master clock. Conversion is initiated by taking $\overline{\text{CONV}}$ low. A conversion lasts 320 master clock cycles, but if $\overline{\text{CONV}}$ is asynchronous to MCLK there may be an uncertainty of 0-4 MCLK cycles after $\overline{\text{CONV}}$ falls to when a conversion actually begins. This may extend the throughput to 324 MCLKs

When the conversion is completed, the output word is placed into the serial port and $\overline{\text{RDY}}$ goes low. To convert continuously, $\overline{\text{CONV}}$ should be held low. In continuous conversion mode with $\overline{\text{CONV}}$ held low, a conversion is performed in 320 MCLK cycles. Alternately $\overline{\text{RDY}}$ can be tied to $\overline{\text{CONV}}$ and a conversion will occur every 322 MCLK cycles.

To perform only one conversion, $\overline{\text{CONV}}$ should return high at least 20 master clock cycles before $\overline{\text{RDY}}$ falls.

Once a conversion is completed and $\overline{\text{RDY}}$ falls, $\overline{\text{RDY}}$ will return high when all the bits of the data word are emptied from the serial port or if the conversion data is not read and $\overline{\text{CS}}$ is held low, $\overline{\text{RDY}}$ will go high two MCLK cycles before the end of conversion. $\overline{\text{RDY}}$ will fall at the end of the next conversion when new data is put into the port register.

See *Serial Port* on page 24 for information about reading conversion data.

Conversion performance can be affected by several factors. These include the choice of clock source for the chip, the timing of $\overline{\text{CONV}}$, and the choice of the serial port mode.

The converter can be operated from an internal oscillator. This clock source has greater jitter than an external crystal-based clock. Jitter may not be an issue when measuring DC signals, or very-low-frequency AC signals, but can become an issue for higher frequency AC signals. For maximum performance when digitizing AC signals, a low-jitter MCLK should be used.

To maximize performance, the $\overline{\text{CONV}}$ pin should be held low in the continuous conversion state to perform multiple conversions, or $\overline{\text{CONV}}$ should occur synchronous to MCLK, falling when MCLK falls.

If the converter is operated at maximum throughput, the SSC serial port mode is less likely to cause interference to measurements as the SCLK output is synchronized to the MCLK. Alternately, any interference due to serial port clocking can also be minimized if data is read in the SEC serial port mode when a conversion is not is progress.

3.3 Clock

The CS5560 can be operated from its internal oscillator or from an external master clock. The state of MCLK determines which clock source will be used. If MCLK is tied low, the internal oscillator will start and be used as the clock source for the converter. If an external CMOS-compatible clock is input into MCLK the converter will power down the internal oscillator and use the external clock. If the MCLK pin is held high, the internal oscillator will be held in the stopped state. The MCLK input can be held high to delete clock cycles to aid in operating multiple converters in different phase relationships.

The internal oscillator can be used if the signals to be measured are essentially DC. The internal oscillator exhibits jitter at about 500 picoseconds rms. If the CS5560 is used to digitize AC signals, an external low-jitter clock source should be used.

If the internal oscillator is used as the clock for the CS5560, the maximum conversion rate will be dictated by the oscillator frequency.

3.4 Voltage Reference

The voltage reference for the CS5560 can range from 2.4 volts to 4.2 volts. A 4.096 volt reference is required to achieve the specified performance. Figure 7 and Figure 8 illustrate the connection of the voltage reference with either a single +5 V analog supply or with ±2.5 V.

For optimum performance, the voltage reference device should be one that provides a capacitor connection to provide a means of noise filtering, or the output should include some type of bandwidth-limiting filter. Some 4.096 volt reference devices need only 5 volts total supply for operation and can be connected as shown in Figure 7 or Figure 8. The reference should have a local bypass capacitor and an appropriate output capacitor.

Some older 4.096 voltage reference designs require more headroom and must operate from an input voltage of 5.5 to 6.5 volts. If this type of voltage reference is used ensure that when power is applied to the system, the voltage reference rise time is slower than the rise time of the V1+ and V1- power supply voltage to the converter. An example circuit to slow the output startup time of the reference is illustrated in Figure 6.

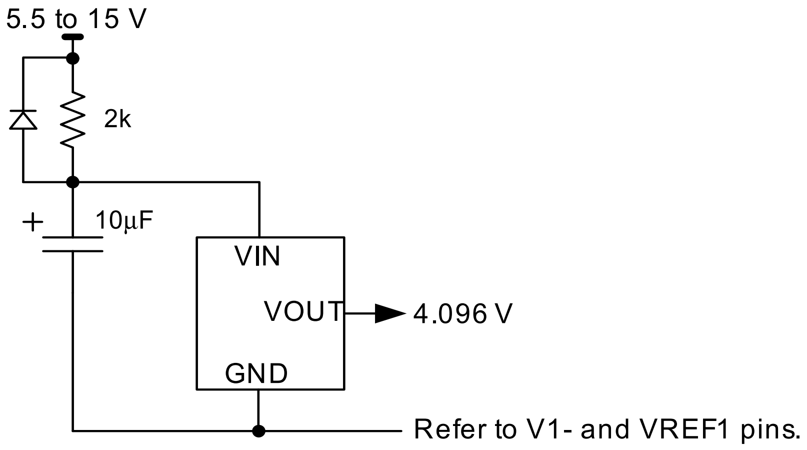


Figure 6. Voltage Reference Circuit

3.5 Analog Input

The analog input of the converter is fully differential with a peak input of 4.096 volts on each input. This is illustrated in Figure 7 and Figure 8. These diagrams also illustrate a differential buffer amplifier configuration for driving the CS5560.

The capacitors at the outputs of the amplifiers provide a charge reservoir for the dynamic current from the A/D inputs while the resistors isolate the dynamic current from the amplifier. The amplifiers can be powered from higher supplies than those used by the A/D but precautions should be taken to ensure that the op amp output voltage remains within the power supply limits of the A/D, especially under start-up conditions.

3.6 Output Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{\text{UP}}$ low), the first code transition occurs 0.5 LSB above zero, and the final code transition occurs 1.5 LSBs below VREF. In the bipolar configuration (BP/$\overline{\text{UP}}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSBs below +VREF. See Table 2 for the output coding of the converter.

Table 2. Output Coding, Two's Complement

Bipolar Input Voltage	Two's Complement
>(VREF-1.5 LSB)	7F FF FF
VREF-1.5 LSB	7F FF FF 7F FF FE
-0.5 LSB	00 00 00 FF FF FF
-VREF+0.5 LSB	80 00 01 80 00 00
<(-VREF+0.5 LSB)	80 00 00

NOTE: VREF = (VREF+) - (VREF-)

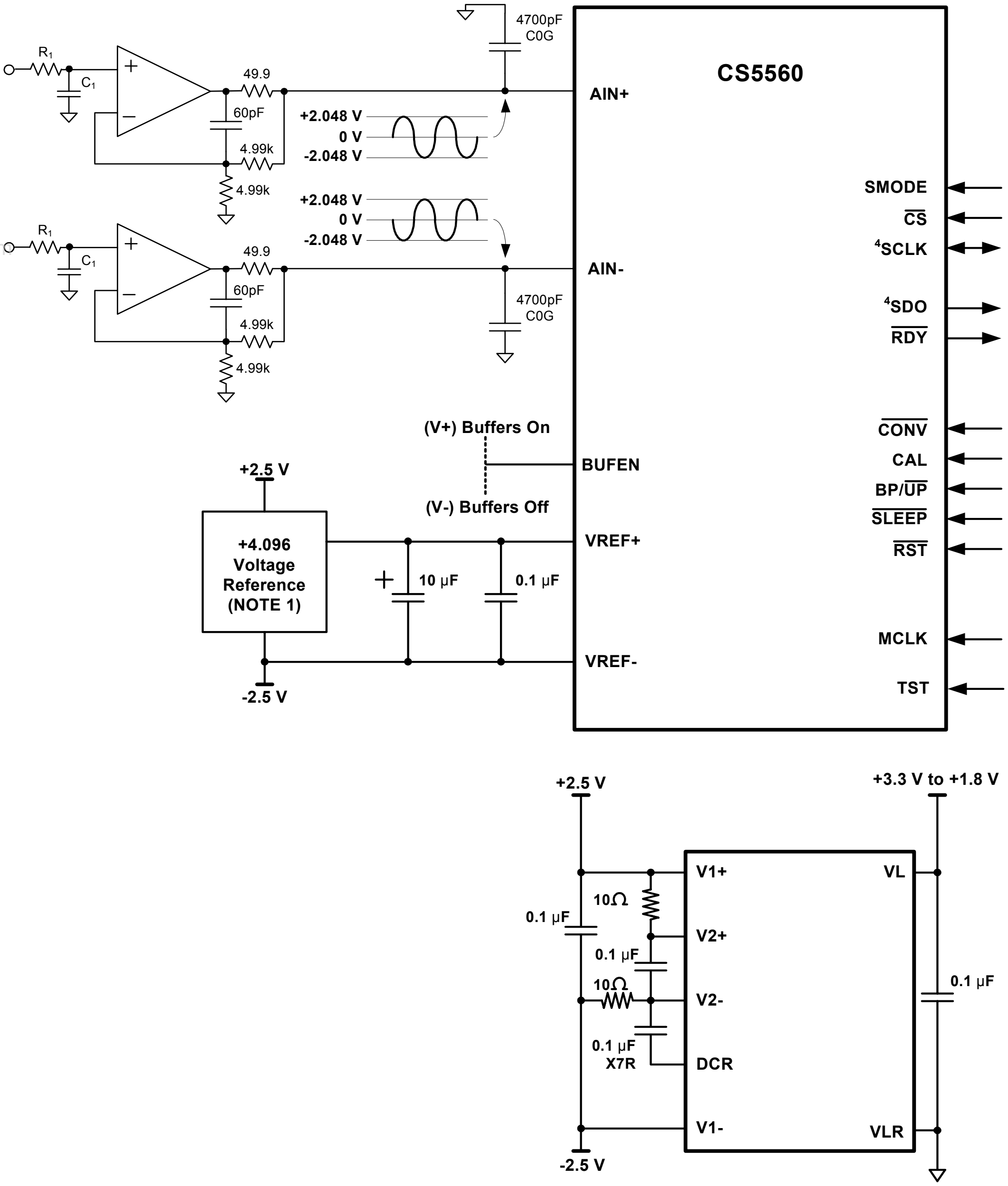
Table 3. Output Coding, Offset Binary

Unipolar Input Voltage	Offset Binary
>(VREF-1.5 LSB)	FF FF FF
VREF-1.5 LSB	FF FF FF FF FF FE
(VREF/2)-0.5 LSB	80 00 00 7F FF FF
+0.5 LSB	00 00 01 00 00 00
<(+0.5 LSB)	00 00 00

NOTE: VREF = (VREF+) - (VREF-)

3.7 Typical Connection Diagrams

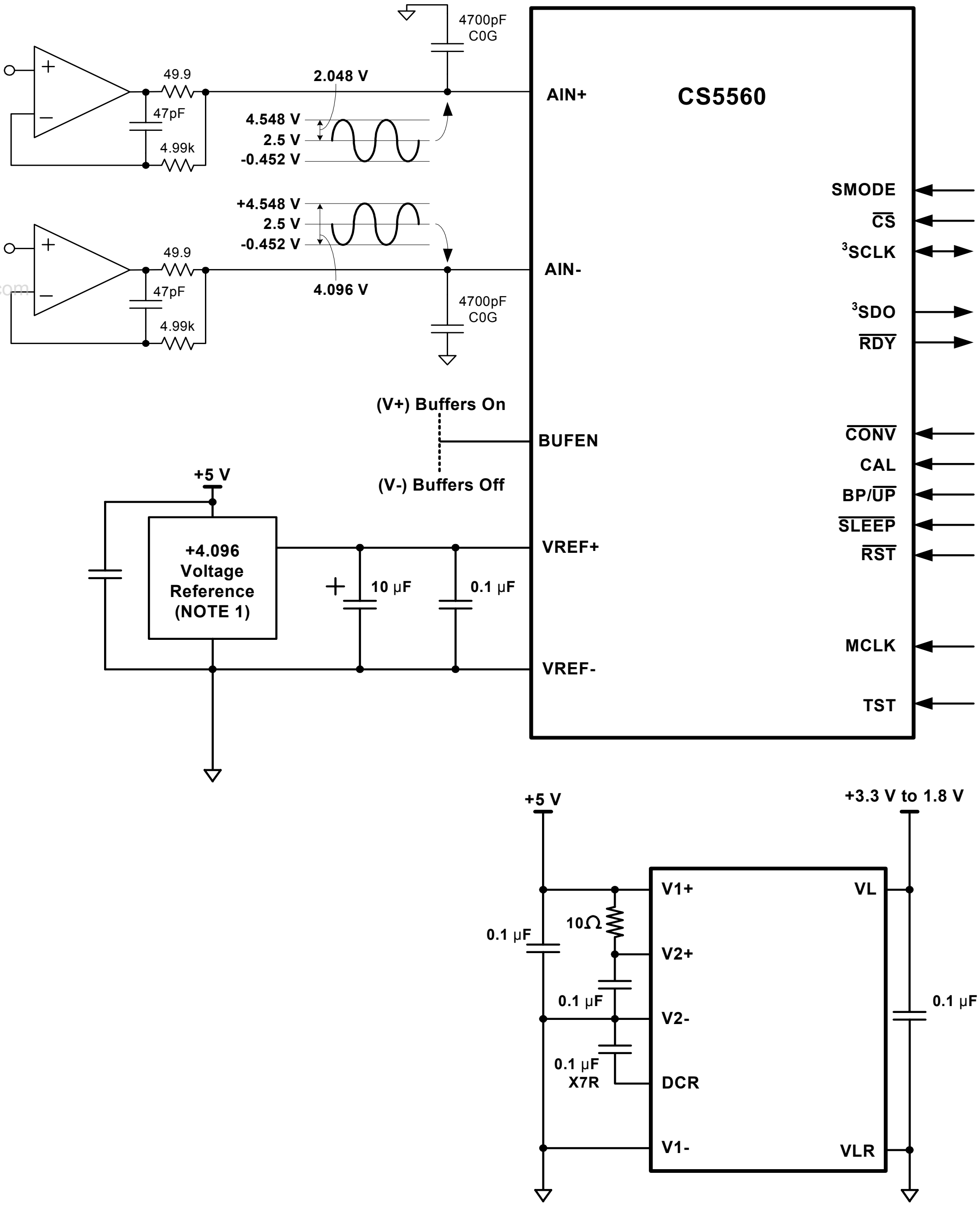
The following figure depicts the CS5560 powered from bipolar analog supplies, +2.5 V and - 2.5 V.



NOTES
1. See Section 3.4 Voltage Reference for information on required voltage reference performance criteria.
2.Locate capacitors so as to minimize loop length.
3. The ±2.5 V supplies should also be bypassed to ground at the converter.
4. VLR and the power supply ground for the ±2.5 V should be connected to the same ground plane under the chip.
5. SCLK and SDO may require pull-down resistors in some applications.
6. An RC input filter can be used to band limit the input to reduce noise. Select R to be equal to the parallel combination of the feedback of the feedback resistors 4.99k || 4.99k = 2.5k))

Figure 7. CS5560 Configured Using ±2.5V Analog Supplies

The following figure depicts the CS5560 device powered from a single 5V analog supply.



NOTES

1. See Section 3.4 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 8. CS5560 Configured Using a Single 5V Analog Supply

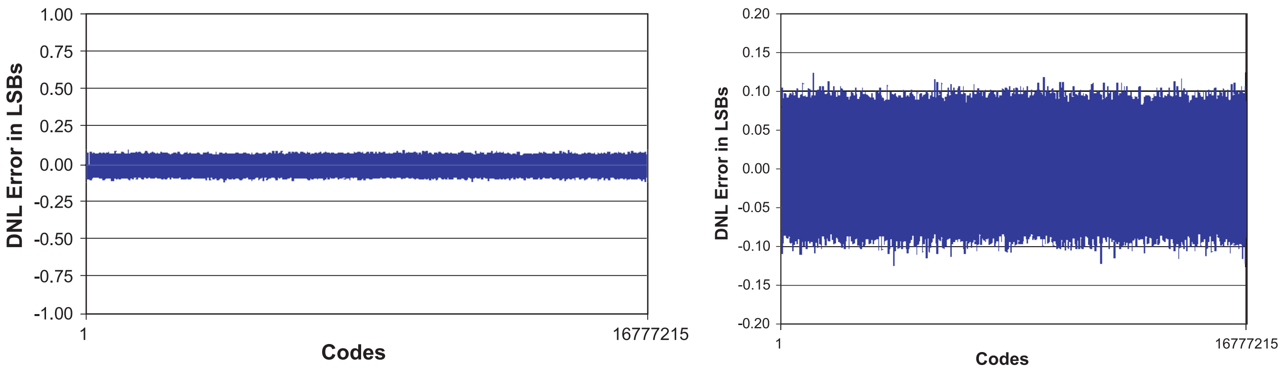
3.8 AIN & VREF Sampling Structures

The CS5560 uses on-chip buffers on the AIN+, AIN-, and the VREF+ inputs. Buffers provide much higher input impedance and therefore reduce the amount of drive current required from an external source. This helps minimize errors.

The Buffer Enable (BUFEN) pin determines if the on-chip buffers are used or not. If the BUFEN pin is connected to the V1+ supply the buffers will be enabled. If the BUFEN pin is connected to the V1- pin the buffers are off. The converter will consume about 30 mW less power when the buffers are off, but the input impedances of AIN+, AIN- and VREF+ will be significantly less than with the buffers enabled.

3.9 Converter Performance

The CS5560 achieves excellent differential nonlinearity (DNL) as shown in Figure 9. Figure 9 illustrates the code widths on the typical scale of ±1 LSB and on a zoomed scale of ±0.2 LSB.



(Zoom View)

Figure 9. CS5560 DNL Plot

3.10 Digital Filter Characteristics

The digital filter is designed for fast settling, therefore it exhibits very little in-band attenuation. The filter attenuation is 1.040 dB at 25 kHz when sampling at 50 kSps.

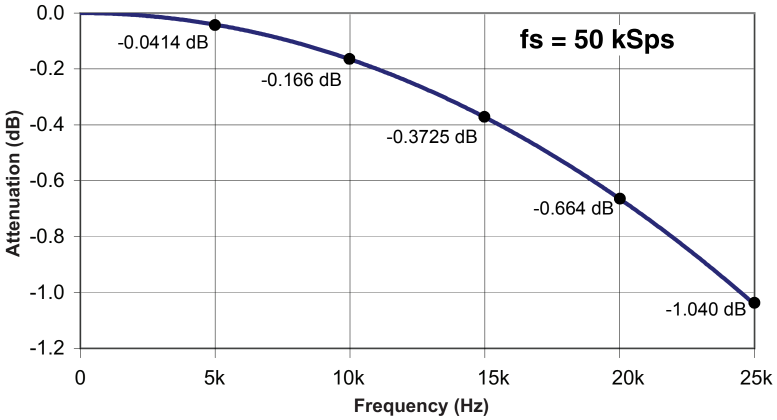


Figure 10. CS5560 Spectral Response (DC to fs/2)

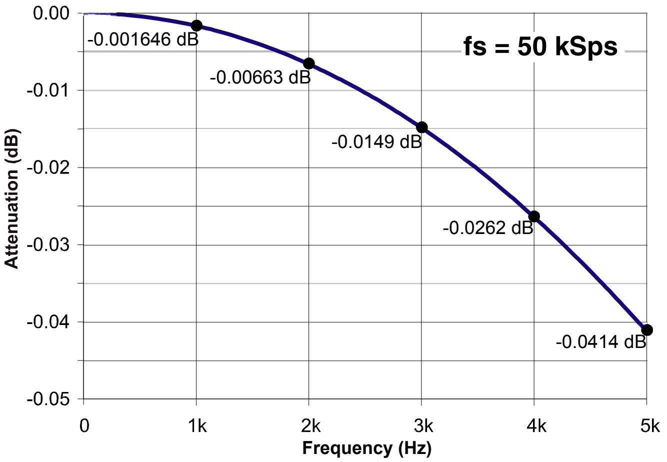


Figure 11. CS5560 Spectral Response (DC to 5 kHz)

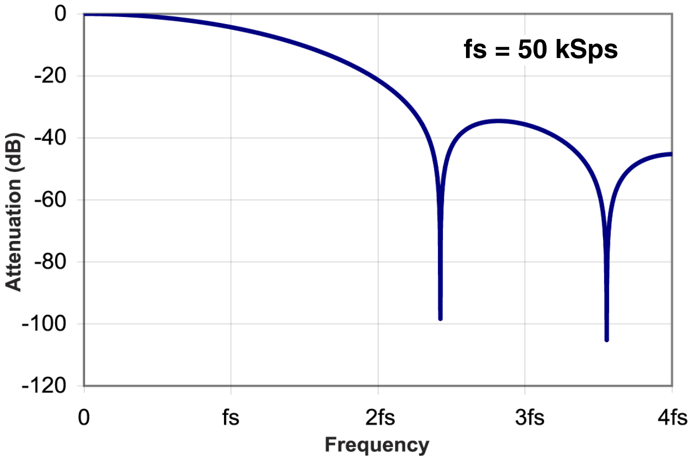


Figure 12. CS5560 Spectral Response (DC to 4fs)

3.11 Serial Port

The serial port on the CS5560 can operate in two different modes: synchronous self clock (SSC) mode & synchronous external clock (SEC) mode. The serial port must be placed into the SEC mode if the offset and gain registers of the converter are to be read or written. The converter must be idle when reading or writing to the on-chip registers.

3.11.1 SSC Mode

If the SMODE pin is high (SMODE = VL), the serial port operates in the SSC (Synchronous Self Clock) mode. In the SSC mode the port shifts out conversion data words with SCLK as an output. SCLK is generated inside the converter from MCLK. Data is output from the SDO (Serial Data Output) pin. If $\overline{\text{CS}}$ is high, the SDO and SCLK pins will stay in a high-impedance state. If $\overline{\text{CS}}$ is low when $\overline{\text{RDY}}$ falls, the conversion data word will be output from SDO MSB first. Data is output on the rising edge of SCLK and should be latched into the external logic on the subsequent rising edge of SCLK. When all bits of the conversion word are output from the port the $\overline{\text{RDY}}$ signal will return to high.

3.11.2 SEC Mode

If the SMODE pin is low (SMODE = VLR), the serial port operates in the SEC (Synchronous External Clock mode). In this mode, the user usually monitors $\overline{\text{RDY}}$. When $\overline{\text{RDY}}$ falls at the end of a conversion, the conversion data word is placed into the output data register in the serial port. $\overline{\text{CS}}$ is then activated low to enable data output. Note that $\overline{\text{CS}}$ can be held low continuously if it is not necessary to have the SDO output operate in the high impedance state. When $\overline{\text{CS}}$ is taken low (after $\overline{\text{RDY}}$ falls) the conversion data word is then shifted out of the SDO pin by driving the SCLK pin from system logic external to the converter. The SDI input must be held low when reading conversion word data. Data bits are advanced on rising edges of SCLK and latched by the subsequent rising edge of SCLK.

If $\overline{\text{CS}}$ is held low continuously, the $\overline{\text{RDY}}$ signal will fall at the end of a conversion and the conversion data will be placed into the serial port. If the user starts a read, the user will maintain control over the serial port until the port is empty. However, if SCLK is not toggled, the converter will overwrite the conversion data at the completion of the next conversion. If $\overline{\text{CS}}$ is held low and no read is performed, $\overline{\text{RDY}}$ will rise just prior to the end of the next conversion and then fall to signal that new data has been written into the serial port.

3.12 Power Supplies & Grounding

The CS5560 can be configured to operate with its analog supply operating from 5V, or with its analog supplies operating from ±2.5V. The digital interface supports digital logic operating from either 1.8V, 2.5V, or 3.3V.

Figure 7 on page 20 illustrates the device configured to operate from ±2.5V analog. Figure 8 on page 21 illustrates the device configured to operate from 5V analog.

To maximize converter performance, the analog ground and the logic ground for the converter should be connected at the converter. In the dual analog supply configuration, the analog ground for the ±2.5V supplies should be connected to the VLR pin at the converter with the converter placed entirely over the analog ground plane.

In the single analog supply configuration (+5V), the ground for the +5V supply should be directly tied to the VLR pin of the converter with the converter placed entirely over the analog ground plane. Refer to Figure 8 on page 21.

3.13 Using the CS5560 in Multiplexing Applications

The CS5560 is a delta-sigma A/D converter. Delta-sigma converters use oversampling as means to achieve high signal to noise. This means that once a conversion is started the converter takes many samples to compute the resulting output word. The analog input for the signal to be converted must remain active during the entire conversion until RDY falls.

The CS5560 can be used in multiplexing applications, but the system timing for changing the multiplexer channel and for starting a new conversion will depend upon the multiplexer system architecture.

The simplest system is illustrated in Figure 13. Any time the multiplexer is changed, the analog signal presented to the converter must fully settle. After the signal has settled, the CONV signal is issued to the converter to start a conversion. Being a delta-sigma converter, the signal must remain present at the input of the converter until the conversion is completed. Once the conversion is completed, RDY falls. At this time the multiplexer can be changed to the next channel and the data can be read from the serial port. The CONV signal should be delayed until after the data is read and until the new analog signal has settled. In this configuration, the throughput of the converter will be dictated by the settling time of the analog input circuit and the conversion time of the converter. The conversion data can be read from the serial port after the multiplexer is changed to the new channel while the analog input signal is settling.

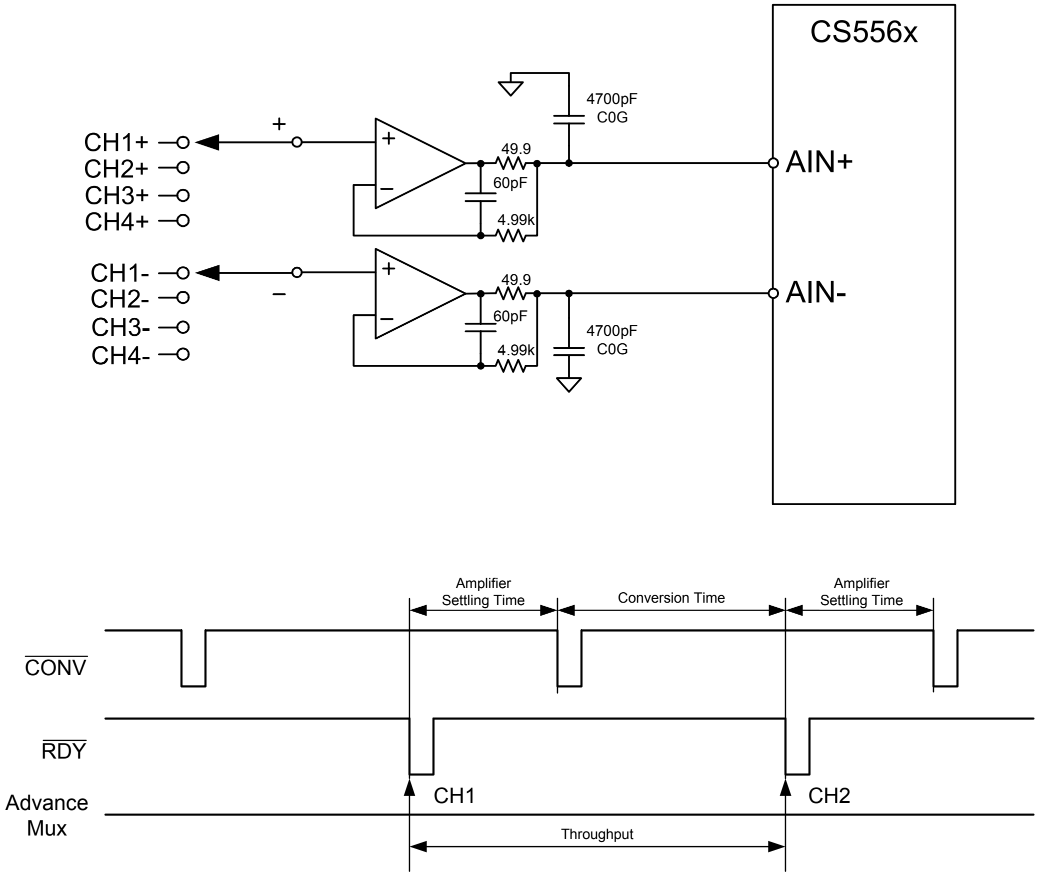


Figure 13. Simple Multiplexing Scheme

A more complex multiplexing scheme can be used to increase the throughput of the converter is illustrated in Figure 14. In this circuit, two banks of multiplexers are used.

At the same time the converter is performing a conversion on a channel from one bank of multiplexers, the second multiplexer bank is used to select the channel for the next conversion. This configuration allows the buffer amplifier for the second multiplexer bank to fully settle while a conversion is being performed on the channel from the first multiplexer bank. The multiplexer on the output of the buffer amplifier and the $\overline{\text{CONV}}$ signal can be changed at the same time in this configuration. This multiplexing architecture allows for maximum multiplexing throughput from the A/D converter.The following figure depicts the recommended analog input amplifier circuit.

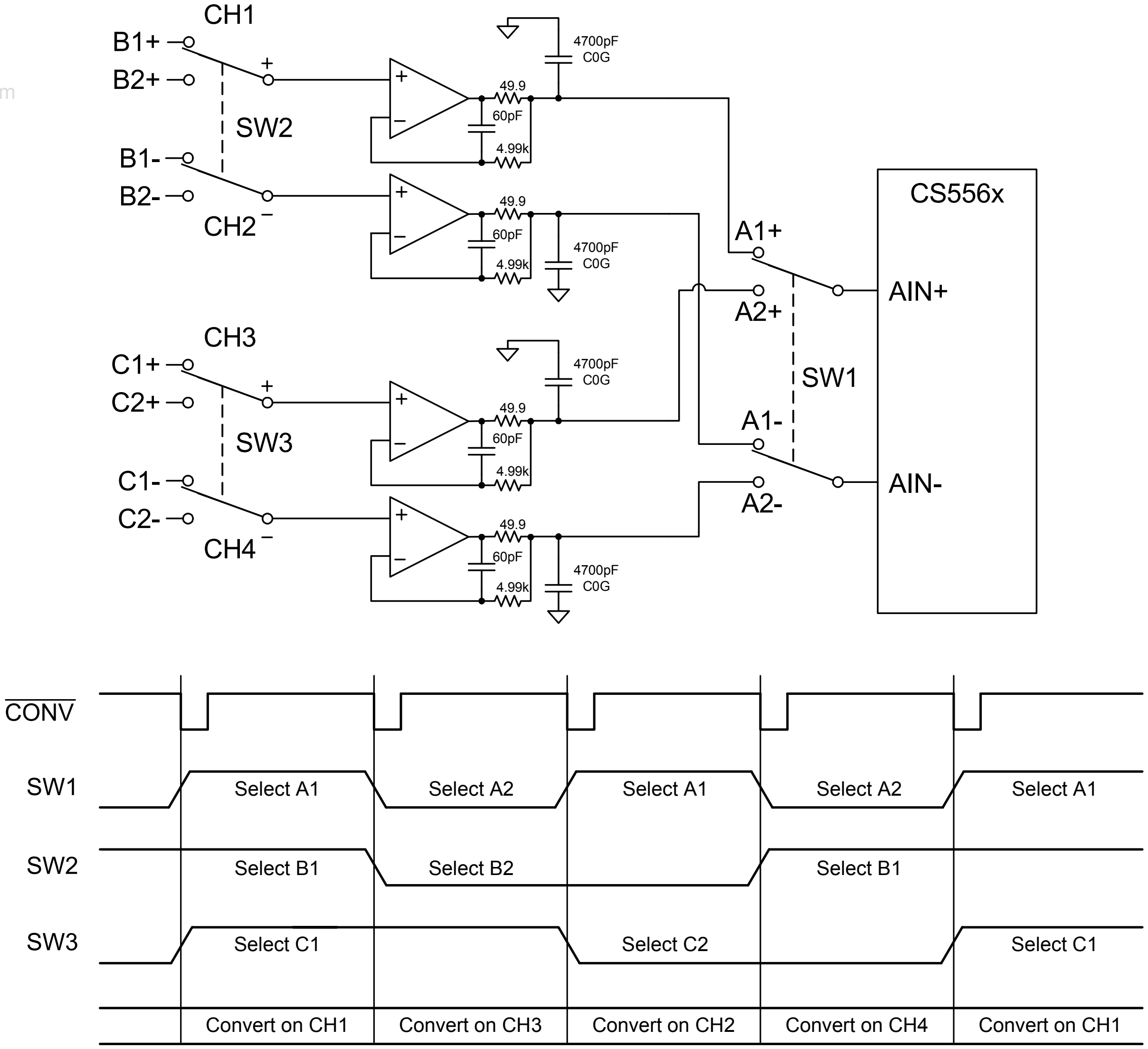
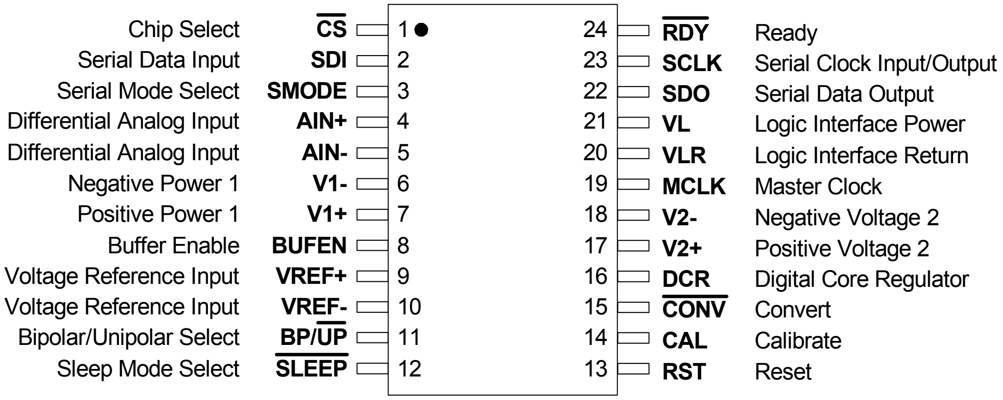


Figure 14. More Complex Multiplexing Scheme

3.14 Synchronizing Multiple Converters

Many measurement systems have multiple converters that need to operate synchronously. The converters should all be driven from the same master clock. In this configuration, the converters will convert synchronously if the same $\overline{\text{CONV}}$ signal is used to drive all the converters, and $\overline{\text{CONV}}$ falls on a falling edge of MCLK. If $\overline{\text{CONV}}$ is held low continuously, reset ($\overline{\text{RST}}$) can be used to synchronize multiple converters if $\overline{\text{RST}}$ is released on a falling edge of MCLK.

4. PIN DESCRIPTIONS



$\overline{\text{CS}}$ – Chip Select, Pin 1

The Chip Select pin allows an external device to access the serial port. If SMODE = VL (SSC Mode) and $\overline{\text{CS}}$ is held high, the SDO output and the SCLK output will be held in a high-impedance output state.

SDI – Serial Data Input, Pin 2

SDI is the input pin for reading and writing calibration registers via the serial port. SDI is only accessible when SMODE is set to enable the SEC serial mode. Data is shifted into this pin by SCLK. SDI should be held low when the serial port is in SSC mode.

SMODE – Serial Mode Select, Pin 3

The serial interface mode pin (SMODE) dictates whether the serial port behaves as a master or slave interface.If SMODE is tied high (to VL), the port will operate in the Synchronous Self-Clocking (SSC) mode. In SSC mode the port acts as a master in which the converter outputs both the SDO and SCLK signals. If SMODE is tied low (to VLR) the port will operate in the Synchronous External Clocking (SEC) mode. In SEC mode, the port acts as a slave in which the external logic or microcontroller generates the SCLK used to output the conversion data word from the SDO pin.

AIN+, AIN- – Differential Analog Input, Pin 4, 5

AIN+ and AIN- are differential inputs for the converter.

V1- – Negative Power 1, Pin 6

The V1- and V2- pins provide a negative supply voltage to the core circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1- and V2- should be supplied from the same source voltage. For single supply operation these two voltages are nominally 0 V (Ground). For dual supply operation they are nominally -2.5 V.

V1+ – Positive Power 1, Pin 7

The V1+ and V2+ pins provide a positive supply voltage to the core circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1+ and V2+ should be supplied from the same source voltage. For single supply operation these two voltages are nominally +5 V. For dual supply operation they are nominally +2.5 V.

BUFEN – Buffer Enable, Pin 8

Buffers on input pins AIN+ and AIN- are enabled if BUFEN is connected to V1+ and disabled if connected to V1-.

VREF+, VREF- – Voltage Reference Input, Pin 9, 10

A differential voltage reference input on these pins functions as the voltage reference for the converter. The voltage between these pins can range between 2.4 volts and 4.2 volts, with 4.096 volts being the nominal reference voltage value.

BP/UP – Bipolar/Unipolar Select, Pin 11

The BP/UP pin determines the span and the output coding of the converter. When set high to select BP (bipolar), the input span of the converter is -4.096 volts to +4.096 volts fully differential (assuming the voltage reference is 4.096 volts) and outputs data is coded in two's complement format. When set low to select UP (unipolar), the input span is 0 to +4.096 fully differential and the output data is coded in binary format.

SLEEP – Sleep Mode Select, Pin 12

When taken low, the SLEEP pin will cause the converter to enter into a low-power state. SLEEP will stop the internal oscillator and power down all internal analog circuitry.

RST – Reset, Pin 13

Reset is necessary after power is initially applied to the converter. When the RST input is taken low, the logic in the converter will be reset. When RST is released to go high, certain portions of the analog circuitry are started. RDY falls when reset is complete.

CAL – Calibrate, Pin 14

After power is applied, a reset should be performed prior to calibration. After an initial reset, calibration can be performed at any time. Calibration can be initiated in either of two ways. If CAL is high when coming out of reset, (RST going high), a calibration will be performed. If RST is taken high with CAL low, a calibration is not performed, but calibration can be initiated by taking CAL high at any time the converter is idle. RDY will also fall when calibration is completed.

CONV – Convert, Pin 15

The CONV pin initiates a conversion cycle if taken low, unless a calibration cycle or a previous conversion is in progress. When the conversion cycle is completed, the conversion word is output to the serial port register and the RDY signal goes low. If CONV is held low and remains low when RDY falls another conversion cycle will be started.

DCR – Digital Core Regulator, Pin 16

DCR is the output of the on-chip regulator for the digital logic core. DCR should be bypassed with a capacitor to V2-. The DCR pin is not designed to power any external load.

V2+ – Positive Power 2, Pin 17

The V1+ and V2+ pins provide a positive supply voltage to the circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1+ and V2+ should be supplied from the same source voltage. For single supply operation these two voltages are nominally +5 V. For dual supply operation they are nominally +2.5 V.

V2- – Negative Power 2, Pin 18

The V1- and V2- pins provide a negative supply voltage to the circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1- and V2- should be supplied from the same source voltage. For single supply operation these two voltages are nominally 0 V (Ground). For dual supply operation they are nominally -2.5 V.

MCLK – Master Clock, Pin 19

The master clock pin (MCLK) is a multi-function pin. If tied low (MCLK = VLR) the on-chip oscillator will be enabled. If tied high (MCLK = VL), all clocks to the internal circuitry of the converter will stop. When MCLK is held high the internal oscillator will also be stopped. MCLK can also function as the input for an external CMOS-compatible clock that conforms to supply voltages on the VL and VLR pins.

VLR, VL – Logic Interface Power/Return, Pin 20, 21

VL and VLR are the supply voltages for the digital logic interface. VL and VLR can be configured with a wide range of common mode voltage. The following interface pins function from the VL/VLR supply: SMODE, $\overline{\text{CS}}$, SCLK, SDI, SDO, $\overline{\text{RDY}}$, $\overline{\text{SLEEP}}$, $\overline{\text{CONV}}$, $\overline{\text{RST}}$, CONV, CAL, BP/$\overline{\text{UP}}$, and MCLK.

SDO – Serial Data Output, Pin 22

SDO is the output pin for the serial output port. Data from this pin will be output at a rate determined by SCLK and in a format determined by the BP/$\overline{\text{UP}}$ pin. Data is output MSB first and advances to the next data bit on the rising edges of SCLK. SDO will be in a high impedance state when $\overline{\text{CS}}$ is high.

SCLK – Serial Clock Input/Output, Pin 23

The SMODE pin determines whether the SCLK signal is an input or an output signal. SCLK determines the rate at which data is clocked out of the SDO pin. If the converter is in SSC mode, the SCLK frequency will be determined by the master clock frequency of the converter (either MCLK or the internal oscillator). In SEC mode, the user determines the SCLK frequency.

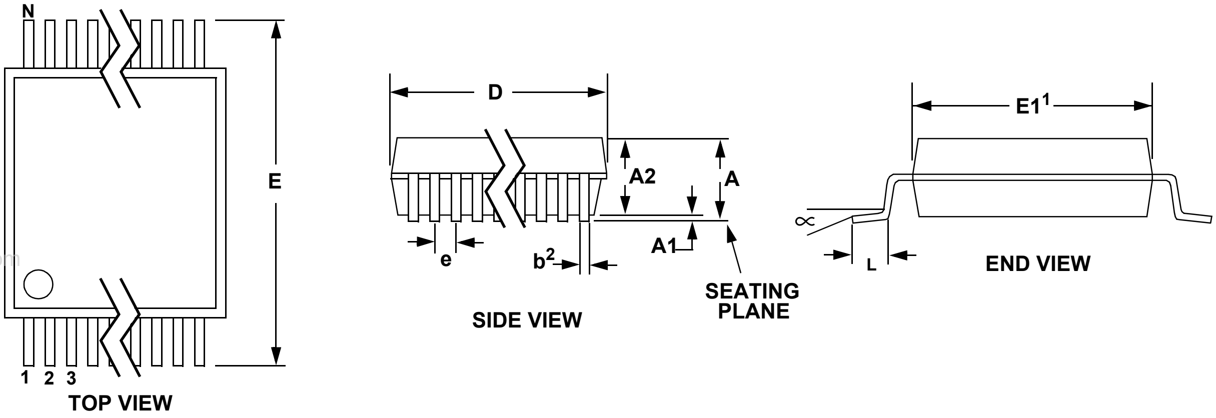
If SMODE = VL (SSC Mode), SCLK will be in a high-impedance state when $\overline{\text{CS}}$ is high.

$\overline{\text{RDY}}$ – Ready, Pin 24

The $\overline{\text{RDY}}$ signal rises when a calibration is initiated. When the calibration is near completion the state of $\overline{\text{CONV}}$ is examined. If $\overline{\text{CONV}}$ is high, the $\overline{\text{RDY}}$ signal will fall upon the completion of calibration. If $\overline{\text{CONV}}$ is low the converter will immediately start a conversion and $\overline{\text{RDY}}$ will remain high until the conversion is completed. At the end of any conversion $\overline{\text{RDY}}$ falls to indicate that a conversion word has been placed into the serial port. $\overline{\text{RDY}}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{\text{CS}}$ pin is inactive (high); or two master clock cycles before new data becomes available if the user holds $\overline{\text{CS}}$ low but has not started reading the data from the converter when in SEC mode.

5. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

6. ORDERING INFORMATION

Model	Linearity	Temperature	Conversion Time	Throughput	Package
CS5560-ISZ	0.0007%	-40 to +85 °C	20 µs	50 kSps	24-pin SSOP

7. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5560-ISZ	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. REVISION HISTORY

Revision	Date	Changes
A1	MAY 2007	Advance release.
A2	JUN 2007	Updated serial interface timing parameters.
A3	JUN 2007	Added DNL plot.
A4	JUN 2007	Updated Typical Connection diagram.
A5	AUG 2007	Corrected liearity spec. in Ordering Information section.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

IMPORTANT NOTICE

"Advance" product information describes products that are in development and subject to development changes.

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